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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,162	03/31/2008	Jorg Behrens	DE03 0414 US1	3846
65913	7590	07/10/2009	EXAMINER	
NXP, B.V.			IM, JUNGHWA M	
NXP INTELLECTUAL PROPERTY & LICENSING				
M/S41-SJ			ART UNIT	PAPER NUMBER
1109 MCKAY DRIVE				2811
SAN JOSE, CA 95131				
			NOTIFICATION DATE	DELIVERY MODE
			07/10/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/581,162	BEHRENS, JORG	
	Examiner	Art Unit	
	JUNGHWA M. IM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 19 March 2009.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-19 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-19 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 31 May 2009 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Base claims 1 and 14 recite the limitation "the open grid structure exposes the silicon substrate to direct contact with the inner connection metallization." Note that it appears that that the invention is regarding a bonding pad structure (interconnection metallization) on the semiconductor substrate comprising a reinforcing structure of an open grid formation. Therefore, it is confusing to understand what it means that the open grid structure exposes the silicon substrate since the instant invention does not disclose this aspect.

Claims 8 and 19 recite the limitation "wherein the open grid structure of the reinforcing system comprises oxide lands formed directly on the doped silicon substrate." It is confusing to understand what it means since the instant invention does not disclose this aspect.

Claim 9 recites that limitation "the open grid structure forms at least one opening within which the inner connection metallization is in direct contact with the doped silicon substrate." It is confusing to understand since it appears the insulating material covers

the opening, therefore the insulating material is in contact with the doped silicon substrate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al. (US 6680545), hereinafter Young in view of Saran et al. (US 6143396), hereafter Saran.

Regarding claims 1 and 9, insofar as understood, Fig. 1 of Young shows a semiconductor component comprising;

a semiconductor chip made of a doped silicon substrate (BJT), which chip is doped into a semiconductor device and structured, and comprises an inner connection metallization (11, 12; bonding pad) in a contact window, and said inner connection metallization of said semiconductor chip is connected to the respective outer connection metallization by a wire bond connection (21, 22),

Fig. 1 of Young shows most aspects of the instant invention except said inner connection metallization of said semiconductor chip comprises a reinforcing system having an open grid structure on the doped silicon substrate with an opening, that is, a

bonding pad on the semiconductor substrate comprising an grid/lattice formation with an opening. Fig. 1 of Saran shows a bonding pad (12) comprises an inner connection metallization in a contact window characterized in that the inner connection metallization comprises a reinforcing system having an open grid structure (30) on the doped silicon substrate (col. 1, lines 10-13). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Saran into the device of Young in order to have the inner connection metallization of the semiconductor chip comprising a reinforcing system with an open grid structure to strengthen the bonding structure.

Regarding claim 14, insofar as understood, Fig. 1 of Young shows discrete semiconductor device comprising:

a silicon substrate having an emitter and a base (col. 4, line 64 - col. 5, line 9);
the emitter having an emitter contact formed thereon, the emitter contact comprising an inner connection metallization (11; pad for emitter) and;
the base having a base contact formed thereon, the base contact comprising an inner connection metallization (11; pad for base);
a leadframe (150) having connection pins (101, 103); and
a bond wire (21, 25) connected between the emitter contact and a connection pin of the leadframe; and
a bond wire (22) connected between the base contact and a connection pin of the leadframe.

Fig. 1 of Young shows most aspects of the instant invention except said inner connection metallization of the emitter and the base of said semiconductor chip comprises a reinforcing system having an open grid structure on the doped silicon substrate with an opening, that is, a bonding pad of the emitter and the base on the semiconductor substrate comprising an grid/lattice formation with an opening. Fig. 1 of Saran shows a bonding pad (12) comprises an inner connection metallization in a contact window characterized in that the inner connection metallization comprises a reinforcing system having an open grid structure (30) on the doped silicon substrate (col. 1, lines 10-13). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Saran into the device of Young in order to have the inner connection metallization of the emitter and the base the semiconductor chip comprising a reinforcing system with an open grid structure to strengthen the bonding structure.

Regarding claims 2, 10 and 15, Fig. 1 of Saran shows the reinforcing system having an open grid structure is formed from an insulation coating (col. 3, lines 16-37).

Regarding claims 3, 11 and 16, Fig. 7 of Saran shows a semiconductor component as claimed in claim 1, characterized in that the grid structure is formed so as to be an open groove structure.

Regarding claims 4, 12 and 17, Fig. 4A of Saran shows a semiconductor component as claimed in claim 1, characterized in that the grid structure may be formed so as to be an open tube structure.

Regarding claims 5, 13 and 18, Fig. 4A of Saran shows a semiconductor component as claimed in claim 1, characterized in that the area of the grid structure of thermal oxide (col. 3, lines 32-38) constitutes >50% of the area of the contact window.

Regarding claim 6, the combination of Young/Saran shows the open grid structure comprise grid lands, however, fails to show “wherein a ratio of height, h, to width, b, of the grid lands is in the range of 1:25 to 1:50.” However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a ratio of height to width of the grid lands in the range of 1:25 to 1:50 to increase the structural reliability, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 7, the combination of Young/Saran shows “the open grid structure comprises grid lands and grid openings,” however, fails to show wherein the ratio between the area of the grid lands and the area of the grid openings is greater than 70%.” However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have the area of the grid openings greater than 70% to adjust the mechanical strength, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claims 8 and 19, insofar as understood, Saran discloses in that the area of the grid structure of thermal oxide the silicon substrate (col. 3, lines 32-38).

Response to Arguments

Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUNGHWA M. IM whose telephone number is (571)272-1655. The examiner can normally be reached on MON.-FRI. 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art
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/J. M. I./
Examiner, Art Unit 2811